50-Gbit/s InP HEMT 4:1 Multiplexer/1:4 Demultiplexer Chip Set With a Multiphase Clock Architecture

Kimikazu Sano, *Member, IEEE*, Koichi Murata, *Member, IEEE*, Hiroto Kitabayashi, Suehiro Sugitani, Hirohiko Sugahara, *Member, IEEE*, and Takatomo Enoki, *Senior Member, IEEE*

***Abstract*—A 50-Gbit/s InP high electron-mobility transistor (HEMT) chip set of 4:1 multiplexer (MUX) and 1:4 demultiplexer (DMUX) integrated circuits (ICs) with a multiphase clock (MPC) architecture is described. The MPC architecture employs a quarter-rate four-phase clock generated by a toggle flip-flop inside the ICs, which reduces the number of circuit elements and lowers the power consumption. The fabricated 4:1 MUX and 1:4 DMUX ICs exhibited 50-Gbit/s error-free operations for $2^{31}-1$ pseudorandom bit sequences with 1.71- and 1.42-W power consumption, respectively. Compared to conventional tree-type 4:1 MUX and 1:4 DMUX ICs using InP HEMTs, the MPC 4:1 MUX and 1:4 DMUX ICs operate at the same operating speed with less than one-third power consumption.**

***Index Terms*—4:1 multiplexer (MUX), InP high electron-mobility transistor (HEMT), multiphase clock (MPC), OC-768, 1:4 demultiplexer (DMUX), optical communication systems, STM-256.**

I. Introduction

OPTICAL communication systems using 40-Gbit/s electrical time-division-multiplexing are being developed to increase the capacity of networks. In 40-Gbit/s systems, 4:1 multiplexer (MUX) and 1:4 demultiplexer (DMUX) integrated circuits (ICs) are key components; they generate a serial 40-Gbit/s data stream from four parallel 10-Gbit/s streams and vice versa. 4:1 MUX ICs operating at over 40 Gbit/s have been demonstrated by using SiGe HBTs [1]–[4], GaAs HBTs [5], GaAs high electron-mobility transistors (HEMTs) [6], InP HBTs [7], [8], and InP HEMTs [9], [10]. As for the 1:4 DMUX ICs, operations over-40-Gbit/s have been reported using SiGe HBTs [1]–[3], InP HBTs [8], [11], [12], and InP HEMTs [10], [13]. With regard to the circuit architectures of the 4:1 MUX and 1:4 DMUX ICs, several ICs incorporate additional functional circuits in addition to the 4:1 multiplexing or 1:4 demultiplexing core circuit. An example of an additional circuit is a clock multiplier unit (CMU) in a 4:1 MUX IC [4], which multiplies a low-input clock rate to the high one needed in the IC. Several 1:4 DMUX ICs [1]–[3] integrate a bit rotation (BR) circuit that can externally control the order of the four output channels. Although there are some differences with respect to the additional circuits, the architectures of 4:1 MUX and 1:4 DMUX core circuits are all the same: a tree-type architecture that uses a recursive series of 2:1 MUX or 1:2 DMUX. A tree-type architecture can be configured with the commonly used differential clocks; however, it requires many circuit elements and tends to consume a lot of power.

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The authors are with the NTT Photonics Laboratories, NTT Corporation, Atsugi-shi, Kanagawa, Japan (e-mail: ksano@aecl.ntt.co.jp).

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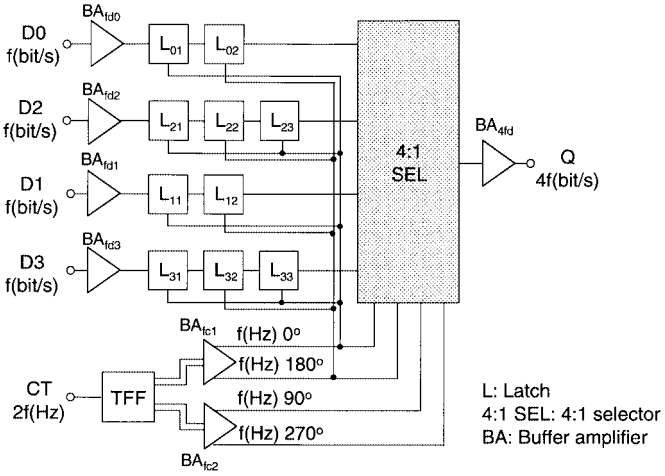

Fig. 1. Circuit block diagram of a 4:1 MUX IC with MPC architecture.

In this paper, an InP HEMT chip set of 4:1 MUX and 1:4 DMUX ICs with a multiphase clock (MPC) architecture is described. The MPC architecture is the one for the 4:1 MUX and 1:4 DMUX core circuit and employs a quarter-rate four-phase clock generated in a toggle flip-flop (TFF), which reduces the number of circuit elements and lowers power consumption. The MPC 4:1 MUX IC exhibited 50-Gbit/s error-free operation for a $2^{31}-1$ pseudorandom bit sequence (PRBS) at 1.71-W power consumption. The MPC 1:4 DMUX IC operated error free for 50-Gbit/s $2^{31}-1$ PRBS and consumed 1.42 W. Compared with conventional tree-type 4:1 MUX and 1:4 DMUX ICs using InP HEMTs, the MPC 4:1 MUX and 1:4 DMUX ICs reduce power consumption to less than one-third while maintaining an operating speed of 50 Gbit/s.

II. Circuit Design

A. 4:1 MUX

Fig. 1 shows the circuit block diagram of the 4:1 MUX IC with MPC architecture. The IC consists of a TFF, which generates a quarter-rate four-phase clock, four parallel latch lines, which deskew the four parallel data inputs and align them with the four-phase clock for 4:1 multiplexing, a series-gated 4:1 selector, which multiplexes the four inputs into a serial stream,

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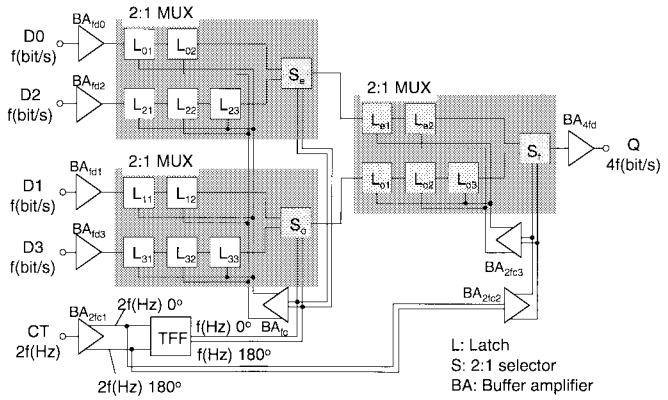


Fig. 2. Circuit block diagram of a 4 : 1 MUX IC with conventional tree-type architecture.

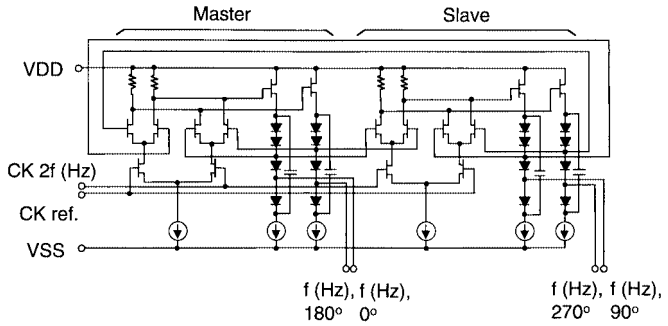


Fig. 3. Circuit diagram of TFF.

and buffer amplifiers, which distribute or output the signals. For comparison, a block diagram of a 4 : 1 MUX IC with the conventional tree-type architecture is shown in Fig. 2. The numbers of circuit elements, including buffers, are 19 for the MPC and 28 for the tree type. Here, the MPC eliminates the circuit elements that handle $2f$-(bit/s) data and $2f$-(Hz) clock, which consume more power than those handling f-(bit/s) data and f-(Hz) clock in order to guarantee $2f$-(bit/s) or $2f$-(Hz) high-speed operation. Therefore, power consumption is reduced substantially for the MPC. In addition, the reduced number of circuit elements makes the chip size smaller. The dotted blocks in Figs. 1 and 2 indicate critical logic elements in the timing design. In these blocks, the timing conditions between the input clock and data are not adjustable externally; therefore, they have to be designed inside the ICs so as to operate correctly [10]. The tree type has eight critical elements. In contrast, the MPC has only one, which simplifies the timing design.

Fig. 3 shows the circuit diagram of the TFF, which is a master–slave type and is operated by the $2f$-(Hz) input clock. Fig. 4 illustrates the timing chart of TFF operation. The master part is toggled by the falling edges of the input clock. After the master part is toggled, the slave part is toggled by the rising edges. As a result, they output f-(Hz) clocks where the output of the master precedes that of the slave by 90° at f (Hz). In addition, the outputs are differential so that a four-phase clock of 0°, 90°, 180°, and 270° at f (Hz) is generated. Fig. 5 shows the circuit diagram of the latch circuit used in the four parallel latch lines. The latch holds and outputs the input data taken in at the rising edge of the input clock during the high level, while

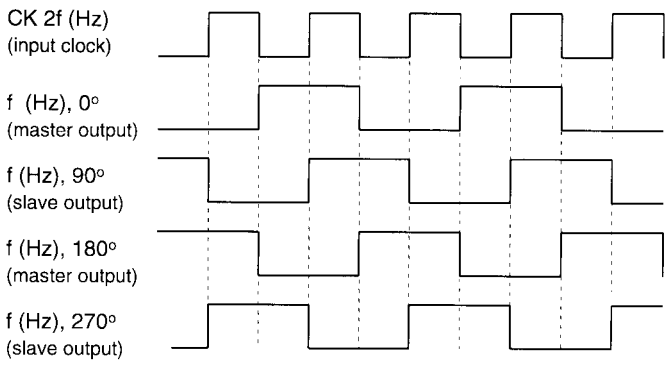


Fig. 4. Timing chart of TFF operation.

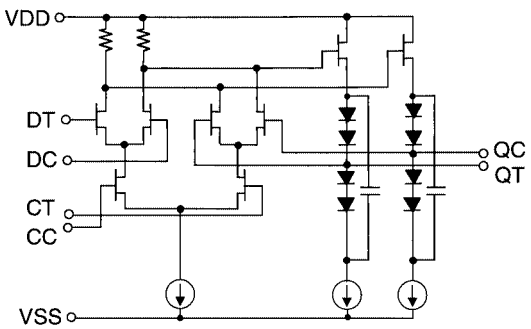


Fig. 5. Circuit diagram of latch circuit.

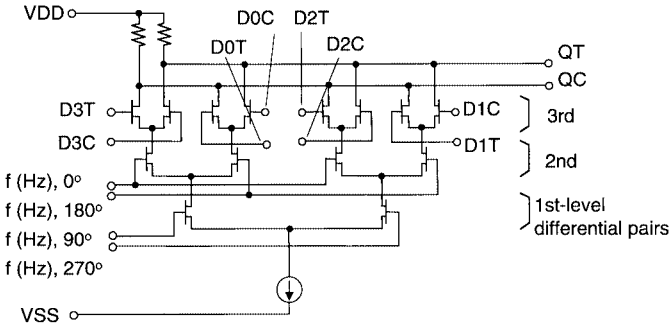


Fig. 6. Circuit diagram of 4 : 1 selector.

it transmits and outputs the input data during the low level. The first latches (L_{01}, L_{11}, L_{21}, and L_{31}) in the four parallel latch lines are driven by the 0° clock, and the second latches (L_{02}, L_{12}, L_{22}, and L_{32}) by the 180° clock. Therefore, all four input data are deskewed at the time of the rising edge of the 0° clock. Moreover, the third latches operated by the 0° clock are added for the latch lines of D2 and D3 so that the outputs of D2 and D3 are delayed by a half-bit behind those of D0 and D1. This alignment of the four data streams provides a wide timing margin in the 4 : 1 multiplexing operation of the 4 : 1 selector, as will be explained in detail below. The 4 : 1 selector (Fig. 6) has three-level series-gated circuitry, where the four-phase clock is input into the first- and second-level differential pairs and the four data streams aligned in the latch lines are input into the third-level pairs. Fig. 7 illustrates the timing chart of 4 : 1 multiplexing in the 4 : 1 selector. The 4 : 1 selector, working in conjunction with the four-phase clock, generates four time-period states, which are expressed using the states of the 0° and 90° clock as $(0°, 90°) = (\text{Low, High})$, (Low,

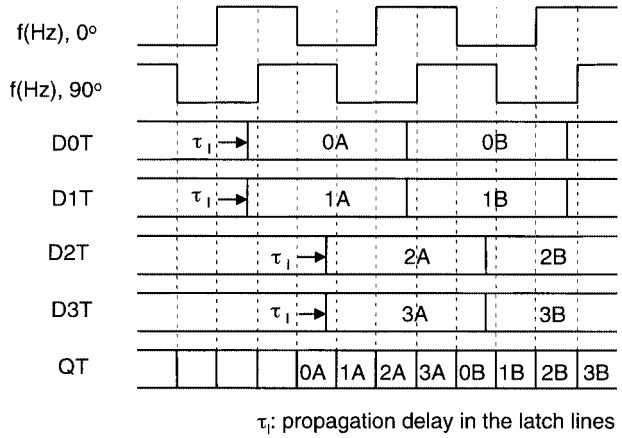


Fig. 7. Timing chart of 4 : 1 multiplexing in 4 : 1 selector.

Low), (High, Low), and (High, High). Each of the four input data is selected and output during one of the four states, i.e., D0, D1, D2, D3, are selected and output during (Low, High), (Low, Low), (High, Low), and (High, High), respectively. This combination of input data and clock states is designed so that the centers of the bit periods of the input data can be selected in consideration of the alignment of the input data and the propagation delays in the latch lines. As a result, a sufficient timing margin between the input data and the four-phase clock is assured. The bit periods of the multiplexed data output in the 4 : 1 selector tend to not be uniform because of the different switching time between the first level differential pairs and the second level pairs, in which the loads are not the same. In order to make the bit periods of the output equal as much as possible, we adjusted the delay time of the four phase clocks so as to compensate for the difference of the switching time by changing the gate delays of the clock buffer amplifiers ($\mathrm{BA_{fc1}}$ and $\mathrm{BA_{fc2}}$) and the lengths of the interconnection lines. The input buffer amplifiers are composed of conventional source followers and differential amplifiers, while the $4f$-(bit/s) output buffer amplifier is equipped with feedback capacitors [14] using drain–source-shortened HEMTs to enhance the bandwidth.

B. 1 : 4 DMUX

Fig. 8 shows the circuit diagram of the 1 : 4 DMUX IC with MPC architecture. The MPC 1 : 4 DMUX IC includes a TFF identical to one in the MPC 4 : 1 MUX IC, four parallel latch lines, which demultiplex a $4f$-(bit/s) input to four parallel f-(bit/s) outputs and deskew the outputs, and buffer amplifiers. For comparison, a block diagram of a 1 : 4 DMUX IC with a conventional tree-type architecture is shown in Fig. 9. The numbers of circuit elements, including the buffer amplifiers, are 20 for the MPC and 25 for the tree type. Like the MPC 4 : 1 MUX IC, circuit elements that handle $2f$-(bit/s) data and $2f$-(Hz) clock are excluded. Therefore, a large power reduction is expected for the MPC 1 : 4 DMUX as well. There are no logic elements in which the timing conditions between the input clock and data are not adjustable externally in the MPC 1 : 4 DMUX IC, whereas the tree type has such elements in the 2 : 4 demultiplexing part (dotted elements in Fig. 9). On the other hand, for the MPC, the clocks distributed to the four

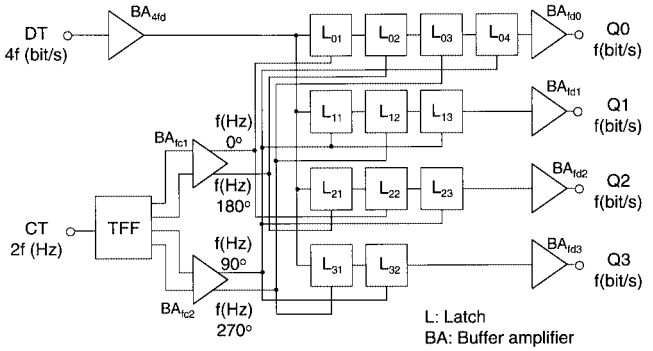


Fig. 8. Circuit block diagram of 1 : 4 DMUX IC with MPC architecture.

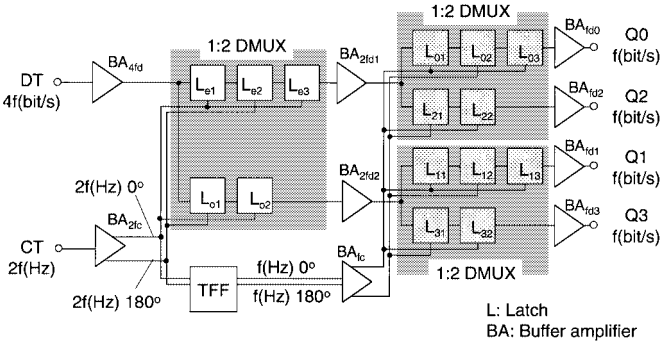


Fig. 9. Circuit block diagram of 1 : 4 DMUX IC with conventional tree-type architecture.

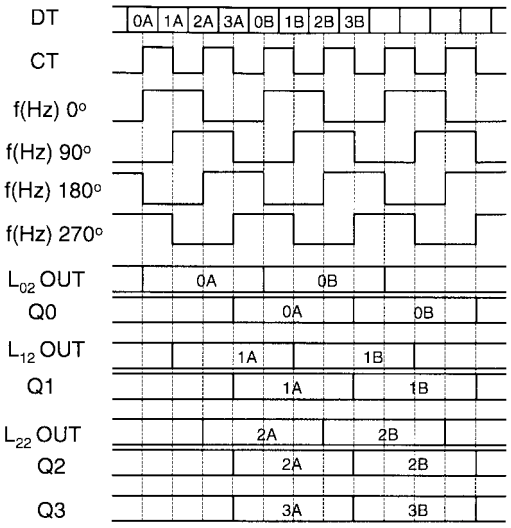
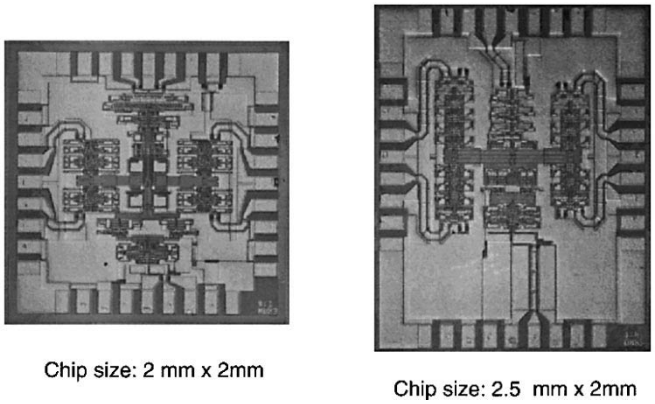


Fig. 10. Timing chart of MPC 1 : 4 DMUX IC.

latch lines must have the precise phase relationship of 0°, 90°, 180°, and 270° in order to achieve a wide phase margin. We designed this phase relationship with an accuracy of ±1 ps by adjusting the gate delays of the clock buffer amplifiers ($\mathrm{BA_{fc1}}$ and $\mathrm{BA_{fc2}}$) and the lengths of the interconnection lines.

The TFF, latch circuits, and buffer amplifiers employed in the MPC 1 : 4 DMUX IC are all identical to those in the MPC 4 : 1 MUX IC. Fig. 10 shows the timing chart of the MPC 1 : 4 DMUX IC. Each of the first latches in the latch lines ($\mathrm{L_{01}}$, $\mathrm{L_{11}}$, $\mathrm{L_{21}}$, and $\mathrm{L_{31}}$) is driven by one of the clocks; i.e., $\mathrm{L_{01}}$, $\mathrm{L_{11}}$, $\mathrm{L_{21}}$,



(a) (b)

Fig. 11. Chip photograph of MPC. (a) 4 : 1 MUX. (b) 1 : 4 DMUX.

and L_{31} are driven by the 0°, 90°, 180°, and 270° clock, respectively. Each latch line thus takes in a different data stream every four bits. For example, the latch line for the Q0 output takes in the data stream 0A, 0B, ... The second latches in the latch lines are driven by the complementary clocks for the first latches. As a result, f-(bit/s) nonreturn to zero (NRZ) data are output in the second latches. Although the 1 : 4 demultiplexing itself is executed only by the first and second latches, there still remains an output phase difference between latch lines, as shown in Fig. 10 (L_{02} OUT, L_{12} OUT, L_{22} OUT, and Q3). To deskew and align the output phases with the 270° clock, the third or the fourth latches, driven by the 270° or 90° clock, are added in the latch lines for the Q0–Q2 output. Consequently, four parallel f-(bit/s) streams aligned with the 270° clock are obtained at the outputs.

III. Fabrication

The chip set of the MPC 4 : 1 MUX and 1 : 4 DMUX ICs was fabricated with 0.1-μm-gate InP HEMTs on a 3-in wafer [15]. Typical transistor parameters of InP HEMTs are transconductance (g_m) of 1.16 S/mm, current cutoff frequency (f_T) of 172 GHz, threshold voltage $(V_{\rm th})$ of −0.49 V, and standard deviation of $V_{\rm th}(\sigma_{V\rm th})$ of 20 mV.

Fig. 11 shows chip photographs of the MPC 4 : 1 MUX and 1 : 4 DMUX ICs. The chip sizes are 2 mm × 2 mm and 2.5 mm × 2 mm for the 4 : 1 MUX and 1 : 4 DMUX, respectively. The numbers of elements are 693 and 769 for the 4 : 1 MUX and 1 : 4 DMUX, respectively. Both the chip sizes and the numbers of elements are almost half those of our previous InP HEMT tree-type 4 : 1 MUX and 1 : 4 DMUX ICs (chip size: 3 mm × 3 mm for both ICs; number of elements: 1327 for the MUX and 1351 for the DMUX) [10]. All inputs are single-ended and terminated with 50-Ω resistors. Clock input is ac coupled, covering above 2 GHz, and data inputs are dc coupled. Output signals are obtained from differential buffer amplifiers; however, for the 4 : 1 DMUX, complementary output ports are terminated with on-chip 50-Ω resistors due to the restriction on the size of the chip.

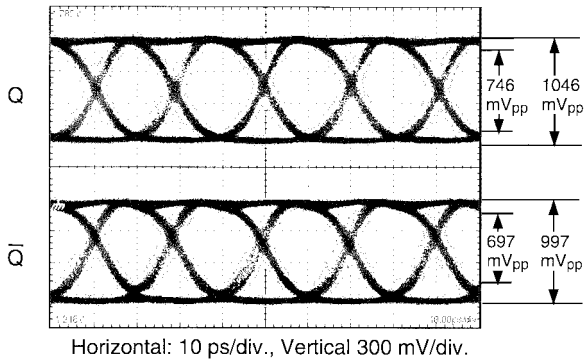


Fig. 12. 50-Gbit/s output waveforms of MPC 4 : 1 MUX IC.

IV. Measurement Results and Discussions

A. 4 : 1 MUX

The MPC 4 : 1 MUX IC was measured on-wafer. We used a four-channel pulse pattern generator (PPG) that operated from 0.1 to 12.5 Gbit/s as a source of the four input data streams, and a synthesizer that output 0.01–50-GHz sinusoidal waves as the input clock source. Since the PPG outputs four-channel PRBSs whose phases are shifted for quarter-PRBS periods between adjacent channels, the multiplexed $4f$-(bit/s) output of the 4 : 1 MUX IC also becomes true PRBS data. The amplitude of all the input data and clock was set to 1 Vpp.

Fig. 12 shows the 50-Gbit/s output waveforms of the IC. Fifty Gbit/s is the upper test bit-rate limit in our setup for true PRBS data, which is limited by the operating range of the PPG. The IC generates a 50-Gbit/s differential signal with clear eye openings. Both of the outputs have ∼1000-mVpp amplitude, ∼700-mVpp eye height, and $a > 15$ Q factor. Power consumption is 1.71 W at −3.8-V supply voltage, which is less than one-third that of the tree-type IC with InP HEMTs (5.47 W) [10]. This drastic reduction in power consumption is due to lower number of circuit elements of the MPC and the lower supply voltage reduced from −4.5 to −3.8 V as a result of optimization. Error-free operation for $2^{31} - 1$ PRBS was confirmed by all four demultiplexed adjacent bits of the MUX output being error free using an InP HEMT delayed flip-flop (D-FF) and an Si bipolar D-FF. The phase margin for the four 12.5-Gbit/s input data was measured by shifting all four data simultaneously, and was approximately 170° (38 ps).

The IC was confirmed to operate through a wide bit-rate range from 7 to 50 Gbit/s. Fig. 13 shows the output waveforms of the IC at 7 Gbit/s (lower limit bit rate of the IC), 40 Gbit/s (close to the STM-256/OC-768 bit rate), and 43 Gbit/s (close to the bit rate of OTU-3, including forward error correcting (FEC) code). For all bit rates, clear eye openings were obtained with ∼1000-mVpp amplitude, ∼800-mVpp eye height, and >17 Q factor. Also, the bit periods (i.e., the bit times) of all eye openings are almost equal. Fig. 14 shows the operating bit-rate dependence of the output eye height for the MPC 4 : 1 MUX and the tree-type 4 : 1 MUX IC [10]. In spite of its low power consumption, the MPC IC exhibits almost the same performance at up to 50 Gbit/s as the tree-type IC.

Fig. 15 summarizes the power consumption and the output amplitude among 4 : 1 MUX ICs reported to operate at

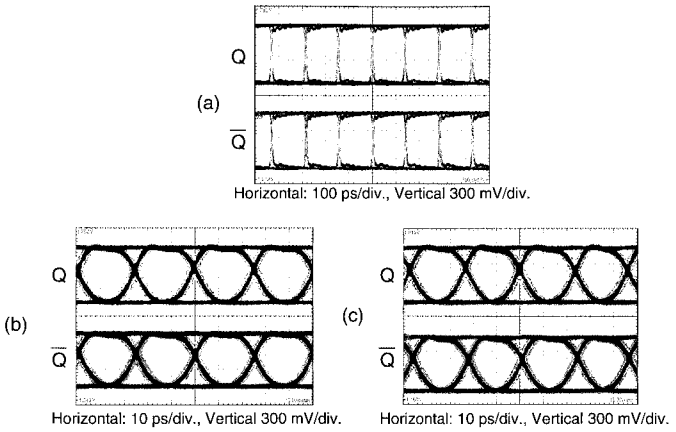


Fig. 13. Output waveforms of MPC 4 : 1 MUX IC at: (a) 7, (b) 40, and (c) 43 Gbit/s.

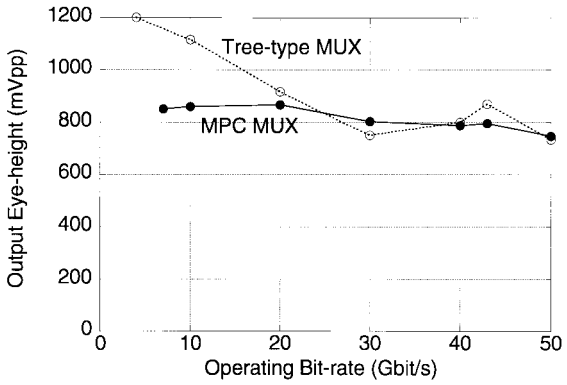


Fig. 14. Operating bit-rate dependence of output eye height of 4 : 1 MUX ICs. Solid: MPC architecture, Dotted: tree-type architecture [10].

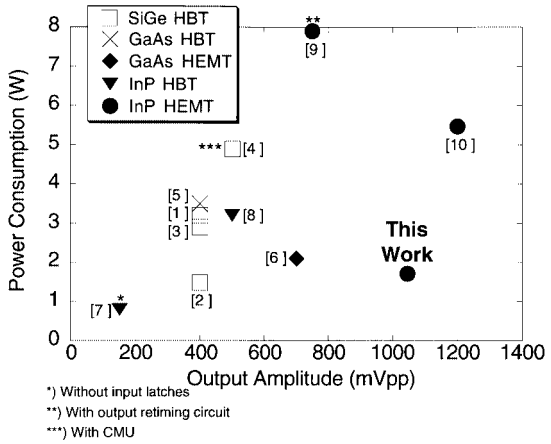


Fig. 15. Power consumption and output amplitude of reported over-40-Gbit/s 4 : 1 MUX ICs.

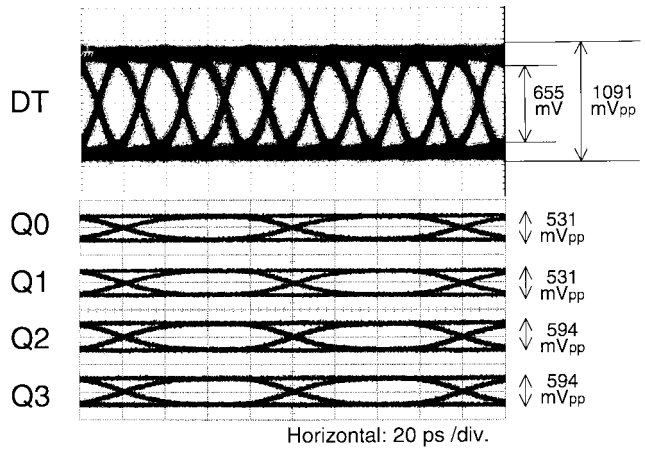


Fig. 16. 50-Gbit/s operating waveforms of MPC 4 : 1 DMUX IC.

over-40 Gbit/s, including this study. InP HEMT 4 : 1 MUX ICs have an advantage in output amplitude, which mitigates the gain requirement for optical modulator driver ICs following the MUX ICs, but they generally consume more power than ICs based on other transistor technologies. The MPC architecture reduces the power consumption of the InP HEMT MUX IC to a level as low as or lower than other technologies while maintaining the larger output.

B. 1 : 4 DMUX

The MPC 1 : 4 DMUX IC was measured on-wafer. The $4f$-(bit/s) input data stream was generated by the combination of the four-channel PPG, a 4 : 2 MUX, and an InP HEMT 2 : 1 MUX. The $2f$-(Hz) input clock was fed from a synthesizer that output a sinusoidal wave. The amplitudes of the input data and clock were 1 Vpp, unless otherwise indicated.

Fig. 16 shows the 50-Gbit/s operating waveforms of the IC. The IC operated error free for $2^{31}-1$ PRBS, where error free means that all four parallel outputs are error free simultaneously and the quarter-PRBS phase shift between adjacent channels is maintained. The phase margin for the error-free operation was 234° (13 ps). The skew of the four parallel outputs at the IC output was below ± 10 ps, which confirms that the output deskew function provided by the four parallel latch lines operates well. The power consumption is 1.42 W at a supply voltage of -3.3 V, which is one-quarter that of the conventional tree-type InP HEMT 1 : 4 DMUX IC (5.53 W) [10]. This drastic reduction is due to the smaller number of elements in the MPC architecture and the lower supply voltage reduced from -4.5 to -3.3 V as a result of optimization. Furthermore, error-free operation was confirmed at supply voltages from -3.0 to -3.8 V. Large tolerance to the variation of the supply voltage is also obtained in spite of the lower power consumption. In the supply voltage range, the power consumption varied from 1.11 (-3.0 V) to 1.86 W (-3.8 V).

The DMUX IC was also tested over a wide range of operating bit rates. Fig. 17 shows the operating bit-rate dependence of the phase margin. For comparison, the dependence for the tree-type IC [10] is also plotted. From 4 to 50 Gbit/s, a phase margin of over 180° was confirmed for both architectures. In spite of the power consumption being as low as one-quarter that of the tree type, the MPC does not sacrifice phase margin, even in high-speed operations at over 40 Gbit/s. Table I shows the input sensitivity of the MPC at 43 and 50 Gbit/s in comparison with that of the packaged tree-type InP HEMT 1 : 4 DMUX IC [10]. For the tree type, the degradation of the input sensitivity due to the insertion loss of the package (2 dB maximum) has to be taken into account; nonetheless, the input sensitivity of the MPC is superior to that of the tree type. We infer that this is also due to the lower power consumption of the MPC since this

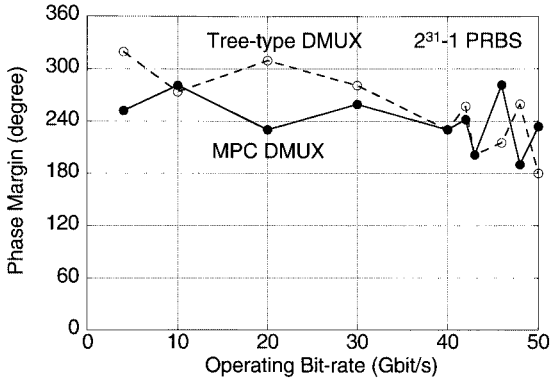


Fig. 17. Operating bit-rate dependence of phase margin of 1 : 4 DMUX ICs. Solid line: MPC architecture. Dotted line: tree-type architecture [10].

TABLE I
INPUT SENSITIVITY OF 1 : 4 DMUX ICS AT 43 AND 50 Gbit/s

Input Sensitivity	MPC DMUX (On-wafer)	Tree-type DMUX (Package)
43 Gbit/s	77 mV (-18.29 dBm)	162 mV (-11.83 dBm)
50 Gbit/s	235 mV (-8.60 dBm)	316 mV (-6.03 dBm)

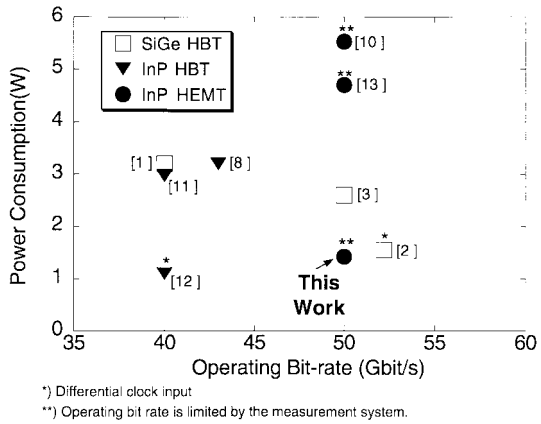


Fig. 18. Power consumption and operating bit rate of reported 40-Gbit/s-class 1 : 4 DMUX ICs.

reduces heat generation and diminishes the noise in the buffer amplifier.

Fig. 18 summarizes the power consumption and the operating bit rate among 1 : 4 DMUX ICs reported for 40-Gbit/s applications, including this study. All of the reported InP HEMT DMUX ICs achieve >50-Gbit/s operation and lead in operating speed. On the other hand, the InP HEMT ICs consume more power than ICs based on SiGe HBTs or InP HBTs. However, the MPC architecture reduces the power consumption of the InP HEMT DMUX IC to a level that is as low as or lower than that of SiGe HBTs and InP HBTs without sacrificing operating speed.

V. CONCLUSION

An InP HEMT chip set of 4 : 1 MUX and 1 : 4 DMUX ICs with MPC architecture has been described. The key feature of the architecture is employment of a quarter-rate four-phase clock generated by a TFF, which reduces the number of circuit elements and lowers the power consumptions of the ICs. The MPC 4 : 1 MUX IC was confirmed to operate from 7 to 50 Gbit/s with an eye height of >700 mVpp at a power consumption of 1.71 W, and the MPC 1 : 4 DMUX IC exhibited error-free operation from 4 to 50 Gbit/s for $2^{31} - 1$ PRBS with $>180^{\circ}$ phase margin and power consumption of 1.42 W. The power consumption of the MPC ICs are less than one-third that of conventional tree-type 4 : 1 MUX and 1 : 4 DMUX ICs. In spite of this drastic power reduction, the output eye height of the MUX IC and the phase margin of the DMUX IC, as well as the operating speed of both ICs, are the same as those of tree-type ICs. This study demonstrates that the MPC architecture can greatly reduce power consumption without sacrificing the operating speed of InP HEMT ICs.

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Kimikazu Sano (M'97) was born in Tokyo, Japan, on September 25, 1971. He received the B.S. and M.S. degrees in electrical engineering from Waseda University, Tokyo, Japan, in 1994 and 1996, respectively.

In 1996, he joined the NTT System Electronics Laboratories, Atsugi, Japan. He is currently with the NTT Photonics Laboratories, NTT Corporation, Atsugi, Kanagawa, Japan. His interest includes ultrafast electronic and opto-electronic circuit design.

Mr. Sano is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 2000 Young Engineer Award presented by the IEICE and the 2003 Young Researcher Award presented at the International Conference on Solid-State Devices and Materials (SSDM).

Koichi Murata (M'92) was born in Osaka, Japan, in 1963. He received the B.S. and M.S. degrees in mechanical engineering from Nagoya University, Nagoya, Japan, in 1987 and 1989, respectively.

He is currently a Senior Research Engineer with the NTT Photonics Laboratories, NTT Corporation, Atsugi, Kanagawa, Japan. He has been engaged in research and development of ultrahigh-speed digital ICs for optical communication systems. His current research interests include opto-electronic IC design and high-speed optical transmission systems.

Mr. Murata is a member of the Institute of Electronics, Information and Communication Engineering (IEICE), Japan.

Hiroto Kitabayashi was born in Tokyo, Japan, on June 2, 1965. He received the B.S. and M.S. degrees in physics from Kyoto University, Kyoto, Japan, in 1990 and 1992, respectively.

In 1992, he joined the NTT LSI Laboratories, Atsugi, Kanagawa, Japan, where he has been engaged in research on epitaxial growth and device physics for resonant interband tunneling diodes. Since 1998, he has studied and developed InP-based heterostructure field-effect transistors and their ICs. He is currently a Senior Research Engineer with the NTT Photonics Laboratories, NTT Corporation, Atsugi, Kanagawa, Japan.

Suehiro Sugitani was born in Kumamoto, Japan, on June 4, 1960. He received the B.E. and M.E. degrees in electronics engineering from Kyushu University, Fukuoka, Japan, in 1983 and 1985, respectively.

In 1985, he joined the NTT Atsugi Electrical Communication Laboratory, Kanagawa, Japan, where he was engaged in research and development on fabrication technology for high-speed GaAs MESFETs and ICs and three-dimensional interconnect technology for GaAs monolithic microwave integrated circuits (MMICs). He is currently engaging in research and development on fabrication technology for ultrahigh-speed InP HEMTs.

Mr. Sugitani is a member of the Japan Society of Applied Physics and the Institute of Electronics, Information and Communication Engineers (IEICE), Japan.

Hirohiko Sugahara (M'93) received the B.S., M.S., and Dr. Eng. degrees in electrical engineering from Waseda University, Tokyo, Japan, in 1980, 1982, and 1998, respectively.

Since 1982, he has been with the NTT Photonics Laboratories, NTT Corporation, Atsugi, Kanagawa, Japan, where he was engaged in research on metal–semiconductor contacts and the GaAs IC reliability. He is currently engaged in the development of InP IC subsystems for high-speed optical communications.

Takatomo Enoki (M'91–SM'01) was born in Tottori, Japan, on November 19, 1959. He received the B.S. and M.S. degrees in physics and the Dr. Eng. degree in electronic and electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1982, 1984, and 1996, respectively.

In 1984, he joined the Atsugi Electrical Communications Laboratories, NTT, Atsugi, Kanagawa, Japan, where he has been engaged in research and development on fabrication technologies for high-frequency and high-speed GaAs MESFETs and ICs. Since 1989, he has studied and developed ultrahigh-speed and low-noise heterostructure FETs and their ICs on an InP substrate. From 1997 to 1999, he was a Senior Manager with the Research Planning Division, after which time he has focused on research and development of ultrahigh-speed heterostructure ICs for optical communications systems with the NTT Photonics Laboratories, NTT Corporation, Atsugi, Kanagawa, Japan. He is currently a Senior Research Engineer, Supervisor and a Research Group Leader in charge of research and development of advanced heterostructure electron devices for future communications.

Dr. Enoki is a member of the Institute of Electronics, Information, and Communication Engineers (IEICE), Japan, the Japan Society of Applied Physics (JSAP), and the Optical Society of America (OSA).